LUMINARY MICRO®

Stellaris® LM3S1968 Evaluation Board

USER'S MANUAL

EK-LM3S1968-02

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CHAPTER 1

Stellaris® LM3S1968 Evaluation Board

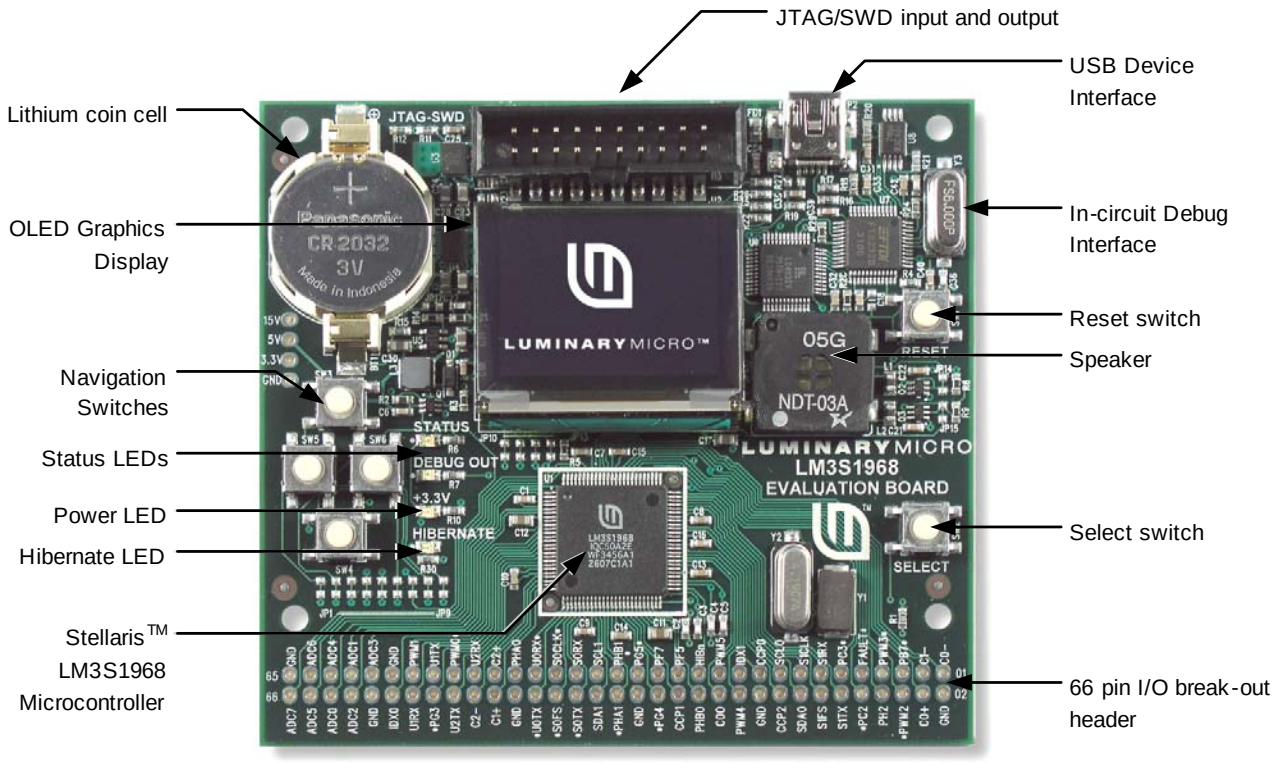
The Stellaris® LM3S1968 Evaluation Board is a compact and versatile evaluation platform for the Stellaris LM3S1968 ARM® Cortex™-M3-based microcontroller. The evaluation kit design highlights the LM3S1968 microcontroller's peripherals and its Hibernation module.

A 3V lithium battery, included in the kit, supplies power to the Hibernation module and maintains data and real-time clock information for about two years in the absence of USB power.

You can use the EVB either as an evaluation platform or as a low-cost in-circuit debug interface (ICDI). In debug interface mode, the on-board microcontroller is disabled, allowing connection of the debug signals to an external Stellaris microcontroller target. The kit is also compatible with high-performance external JTAG debuggers.

This evaluation kit enables quick evaluation, prototype development, and creation of application-specific designs using the LM3S1968's broad range of peripherals. The kit also includes extensive source-code examples, allowing you to start building C code applications quickly.

Figure 1-1. Stellaris LM3S1968 Evaluation Board Layout



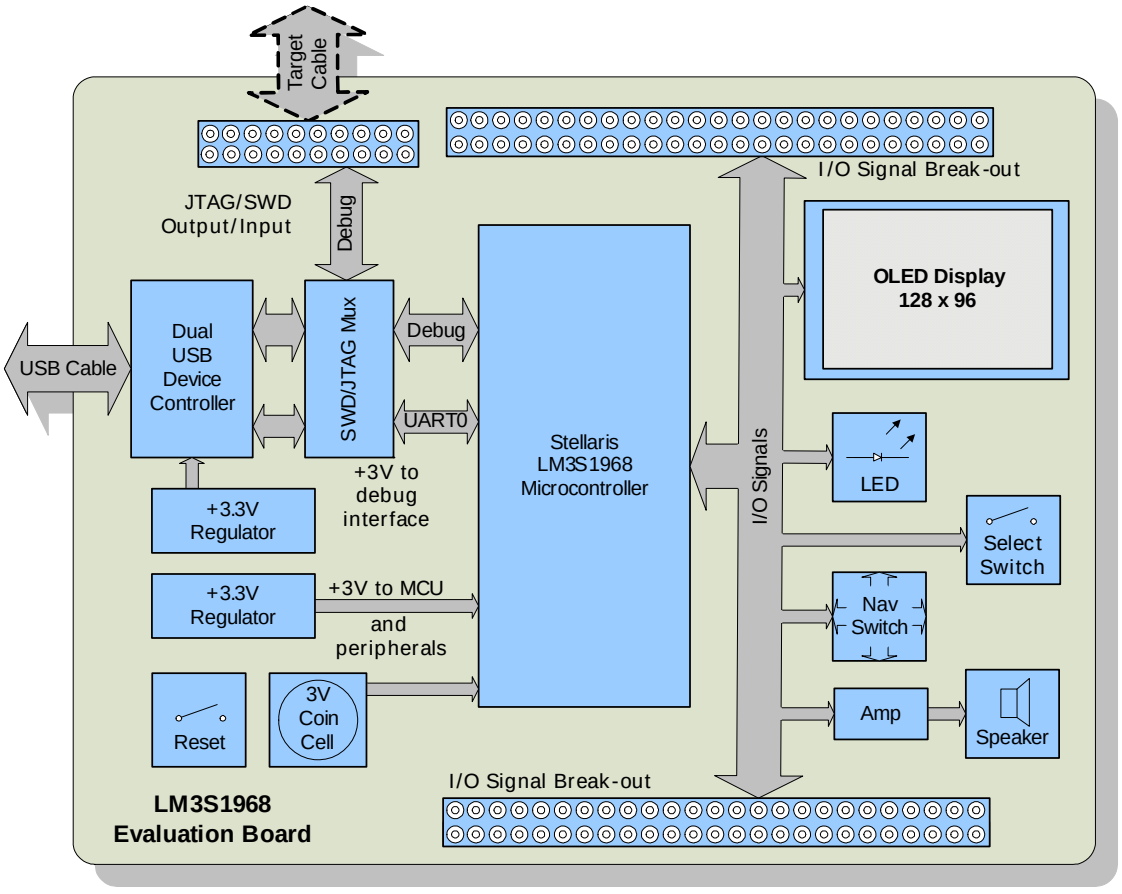
Features

The Stellaris LM3S1968 Evaluation Kit includes the following features:

- Stellaris LM3S1968 microcontroller
- Simple setup; USB cable provides serial communication, debugging, and power
- OLED graphics display with 128 x 96 pixel resolution
- User LED, navigation switches, and select pushbuttons
- 8Ω magnetic speaker with class D amplifier
- Internal 3 V battery and support for on-chip hibernation module
- USB interface for debugging and power supply
- Standard ARM® 20-pin JTAG debug connector with input and output modes
- LM3S1968 I/O available on labeled break-out pads

Block Diagram

Figure 1-2. LM3S1968 Evaluation Board Block Diagram



Evaluation Kit Contents

The evaluation kit contains everything needed to develop and run applications for Stellaris microcontrollers including:

- LM3S1968 evaluation board (EVB)
- USB cable
- 20-pin JTAG/SWD target cable
- CD containing:
  - A supported version of one of the following:
    - Keil™ RealView® Microcontroller Development Kit (MDK-ARM)
    - IAR Embedded Workbench
    - Code Sourcery GCC development tools
    - Code Red Technologies development tools
  - Complete documentation
  - Quickstart guide
  - Quickstart source code
  - Stellaris Firmware Development Package with example source code

Evaluation Board Specifications

- Board supply voltage: 4.37–5.25 Vdc from USB connector
- Board supply current: 130 mA typ (fully active, CPU at 50 MHz)
17 uA (hibernate mode, operating from battery)
- Break-out power output: 3.3 Vdc (60 mA max), 15 Vdc (15 mA max)
- Speaker power: 0.3 W max
- Dimensions: 3.20” x 3.50” x 0.5” (LxWxH)
- RoHS status: Compliant

Features of the LM3S1968 Microcontroller

- 32-bit RISC performance using ARM® Cortex™-M3 v7M architecture
  - 50-MHz operation
  - Hardware-division and single-cycle-multiplication
  - Integrated Nested Vectored Interrupt Controller (NVIC)
  - 42 interrupt channels with eight priority levels
- 256-KB single-cycle Flash
- 64-KB single-cycle SRAM
- Four general-purpose 32-bit timers
- Three fully programmable 16C550-type UARTs
- Eight 10-bit ADC channels (inputs) when used as single-ended inputs

- Three independent integrated analog comparators
- Two I^2C modules
- Three PWM generator blocks
  - One 16-bit counter
  - Two comparators
  - Produces two independent PWM signals
  - One dead-band generator
- Two QEI modules with position integrator for tracking encoder position
- 5 to 52 GPIOs, depending on user configuration
- On-chip low drop-out (LDO) voltage regulator
- Hibernation module

CHAPTER 2

Hardware Description

In addition to a microcontroller, the Stellaris LM3S1968 evaluation board includes a range of useful peripherals and an integrated in-circuit debug interface (ICDI). This chapter describes how these peripherals operate and interface to the microcontroller.

LM3S1968 Evaluation Board

LM3S1968 Microcontroller Overview

The heart of the EVB is a Stellaris LM3S1968 ARM Cortex-M3-based microcontroller. The LM3S1968 offers 256-KB Flash memory, 50-MHz operation, and a wide range of peripherals. Refer to the LM3S1968 data sheet (order number DS-LM3S1968) for complete device details.

The LM3S1968 microcontroller is factory programmed with a quickstart demo program. The quickstart program resides in the LM3S1968 on-chip Flash memory and runs each time power is applied unless the quickstart has been replaced with a user program.

Hibernation Module

The Hibernation Module manages removal and restoration of power to the microcontroller and peripherals while maintaining a real-time clock (RTC) and non-volatile memory. The EVB includes a 3 V Lithium battery to maintain Hibernate module power when USB power is unavailable.

The Hibernation state is initiated in software. Leaving Hibernation mode requires either an RTC timer match event or assertion of the $\overline{\text{WAKE}}$ signal. Pressing the Select switch on the EVB asserts $\overline{\text{WAKE}}$. The Hibernate LED (LED4) signals that the EVB is in Hibernate state (+3.3 V disabled) as long as USB power is present. When USB power is removed, the EVB will remain in the Hibernate state, however, the LED will not be on.

Clocking

The EVB uses an 8.0-MHz crystal to complete the LM3S1968 microcontroller's main internal clock circuit. An internal PLL, configured in software, multiples this clock to 50 MHz for core and peripheral timing.

The real-time clock oscillator is part of the microcontroller's Hibernation module and uses a 4.194304 MHz crystal for timing. This frequency divides by 128 to generate a 32.7680 kHz standard timing frequency.

Reset

The LM3S1968 microcontroller shares its external reset input with the OLED display. In the EVB, reset sources are gated through the CPLD, though in a typical application a simple wired-OR arrangement is sufficient.

External reset is asserted (active low) under any one of three conditions:

- Power-on reset
- Reset push switch SW1 held down

- Internal debug mode—By the USB device controller (U5 FT2232) when instructed by debugger

The LM3S1968 microcontroller has an internal power-on reset, so the external circuits used in the EVB are not required in typical applications.

Power Supplies

In normal operating mode, the LM3S1968 is powered from a +3.3-V supply. A low drop-out (LDO) regulator converts +5-V power from the USB cable to +3.3-V. +3.3-V power is available for powering external circuits.

If +5-V is removed, the Hibernation module will remain powered by the 3-V lithium battery. Other microcontroller and board functions will not function until power is restored.

+15-V power is available when the OLED display power supply is active. The speaker and OLED display boost-converter operate directly from the +5-V power.

Debugging

Stellaris microcontrollers support programming and debugging using either JTAG or SWD. JTAG uses the signals TCK, TMS, TDI, and TDO. SWD requires fewer signals (SWCLK, SWDIO, and, optionally, SWO, for trace). The debugger determines which debug protocol is used. For example, Keil RealView tools support only JTAG debugging.

The JTAG $\overline{\text{TRST}}$ signal is not required for debugging and is not connected to the 20-pin JTAG/SWD header. $\overline{\text{TRST}}$ may be asserted by the CPLD in debug Mode 2.

Debugging Modes

The LM3S1968 evaluation board supports a range of hardware debugging configurations. Table 2-1 summarizes these configurations.

Table 2-1. Stellaris LM3S1968 Evaluation Board Hardware Debugging Configurations

Mode	Debug Function	Use	Selected by
1	Internal ICDI	Debug on-board LM3S1968 microcontroller over USB interface.	Default mode
2	ICDI out to JTAG/SWD header	The EVB is used as a USB to SWD/JTAG interface to an external target.	Connecting to an external target and starting debug software. The red Debug Out LED will be ON.
3	In from JTAG/SWD header	For users who prefer an external debug interface (ULINK, JLINK, etc.) with the EVB.	Connecting an external debugger to the JTAG/SWD header

Modes 2 and 3 automatically detect the presence of an external debug cable. When the debugger software connected to the EVB's USB controller the EVB automatically selects Mode 2 and illuminates the red Debug Out LED.

Debug In Considerations

Debug Mode 3 supports evaluation board debugging using an external debug interface. Mode 3 is automatically selected when a device such as a Segger J-Link or Keil ULINK is connected.

Boards marked Revision B or later automatically configure pin 1 to be a 3.3-V reference, if an external debugger is connected. To determine the revision of your board, locate the product number on the bottom of the board; for example, EK-LM3S6965-B. The last character of the product number identifies the board revision.

A configuration or board-level change may be necessary when using an external debug interface with revision A of this evaluation board. Because the evaluation board supports both debug out and debug in modes, pin 1 of the 20-pin JTAG/SWD header is, by default, not connected to +3.3 V. Consequently, devices requiring a voltage on pin 1 to power their line buffers may not work.

Two solutions exist. Some debugger interfaces (such as ULINK) have an internal power jumper that, in this case, should be set to internal +3.3-V power. Refer to debugger interface documentation for full details. However, if your debugger interface does not have a selectable power source, it may be necessary to install a 0-Ω resistor on the evaluation board to route power to pin 1. Refer to the schematics and board drawing in the appendix of this manual for the location of this resistor.

USB Device Controller Functions

USB Overview

An FT2232 device from Future Technology Devices International Ltd manages USB-to-serial conversion. The FT2232 is factory-configured by Luminary Micro to implement a JTAG/SWD port (synchronous serial) on channel A and a Virtual COM Port (VCP) on channel B. This feature allows two simultaneous communications links between the host computer and the target device using a single USB cable. Separate Windows drivers for each function are provided on the Documentation and Software CD.

A small serial EEPROM holds the FT2232 configuration data. The EEPROM is not accessible by the LM3S1968 microcontroller.

For full details on FT2232 operation, go to www.ftdichip.com.

USB to JTAG/SWD

The FT2232 USB device performs JTAG/SWD serial operations under the control of the debugger. A CPLD (U6) multiplexes SWD and JTAG functions and, when working in SWD mode, provides direction control for the bidirectional data line. The CPLD also implements logic to select between the three debug modes. The target microcontroller selection is determined by multiplexing TCK/SWCLK and asserting $\overline{\text{TRST}}$.

In Hibernate state, the JTAG/SWD interface circuit remains powered. Although debugging is not possible, maintaining power avoids re-enumeration of the USB device after each wake transition. To avoid powering the microcontroller, the CPLD sets its output signals to a high-impedance state whenever the Hibernation signal is asserted.

Virtual COM Port

The Virtual COM Port (VCP) allows Windows applications (such as HyperTerminal) to communicate with UART0 on the LM3S1968 over USB. Once the FT2232 VCP driver is installed, Windows assigns a COM port number to the VCP channel.

Serial Wire Out

The evaluation board supports the Cortex-M3 serial-wire output (SWO) trace capabilities. Under debugger control, the CPLD can route the SWO datastream to the virtual communication port (VCP) transmit channel. The debugger can then decode and interpret the trace information received from the VCP. The normal VCP connection to UART0 is interrupted when using SWO. Not all debuggers support SWO. Refer to the Stellaris LM3S3748 data sheet for additional information on the trace port interface unit (TPIU).

Organic LED Display

The EVB features an Organic LED (OLED) graphics display with 128 x 96 pixel resolution. OLED is a new technology that offers many advantages over LCD display technology. The display is protected during shipping by a thin, protective plastic film. The film can be removed using a pair of tweezers.

Features

- RiT Display P14201 series display
- 128 columns by 96 rows
- High-contrast (typ. 500:1)
- Excellent brightness (120 cd/m^2)
- Fast 10 us response

Control Interface

The OLED display has a built-in controller IC with synchronous serial and parallel interfaces. Synchronous serial (SSI) is used on the EVB as it requires fewer microcontroller pins. Data cannot be read from the OLED controller; only one data line is necessary. The Stellaris® Firmware Development Package (included on the Documentation and Software CD) contains complete drivers with source-code for the OLED display.

Power Supply

A +15-V supply is needed to bias the OLED display. A FAN5331 device from Fairchild combines with a few external components to complete a boost converter. A GPIO (PH3/FAULT) is assigned to turn on and off the controller as necessary for power rail sequencing. When the OLED display is operating, a small amount of power can be drawn from the +15-V supply to power other devices.

Design Guidelines

The OLED display has a lifetime of about 13,000 hours. It is also prone to degradation due to burn-in, similar to CRT and plasma displays. The quickstart application includes both a screen saver and a power-down mode to extend display life. These factors should be considered when developing EVB applications that use the OLED display.

Further Reference

For additional information on the RiT OLED display, visit www.ritekdisplay.com.

Other Peripherals

Speaker

The LM3S1968 evaluation board's speaker circuit can be used in either tone or waveform mode. The quick-start application uses tone mode.

In tone mode, the LM3S1968 microcontroller's PWM module directly generates tones within the audible frequency range. The width of the pulses determines the volume. If only one PWM signal (PWM2 or PWM3) is used, the non-PWM signal should be configured as a general-purpose output. For increased speaker volume, PWM2 and PWM3 can be configured as complementary drive signals. In tone mode, be careful to avoid large DC currents in the speaker.

Waveform mode uses two high-frequency PWM signals to drive a MOSFET H-bridge with an output filter. This circuit is essentially a Class-D amplifier. The symmetrical 2nd order low-pass L-C filter has a cut-off frequency of approximately 33 kHz. The microcontroller's PWM module should be configured with a PWM frequency of at least 100 kHz. Using 500 kHz improves audio quality even further. Once configured, audio waveform data can be used to update the PWM duty cycle at a rate equal to the audio sampling rate.

The speaker on the evaluation board has standard 8Ω impedance. Audio quality can be enhanced by adding a small, vented enclosure around the speaker.

Push Switches

The EVB has five general-purpose input switches. Four are arranged in a navigation-style configuration. The fifth functions as a Select switch on PG7. The Select switch also connects to the $\overline{\text{WAKE}}$ signal of the Hibernate module which has an internal pull-up resistor. A diode (D2) blocks current into the PG7 pin when in the Hibernate state.

User LED

A user LED (LED3) is provided for general use. The LED is connected to PG2/PWM0, allowing the option of either GPIO or PWM control (brightness control). Refer to the Quickstart Application source code for an example of PWM control.

Bypassing Peripherals

The EVB's on-board peripheral circuits require 15 GPIO lines. This leaves 31 GPIO lines and 8 ADC channels immediately available for connection to external circuits. If an application requires more GPIO lines, the on-board hardware can be disconnected. The EVB is populated with 15 jumper links, which can be cut with a knife to isolate on-board hardware. The process can be reversed by installing 0603- 0-ohm chip resistors. Table 2-2 shows the microcontroller assignments and how to isolate specific pins.

Important: The quickstart application will not run if one or more jumpers are removed.

Table 2-2. Isolating On-Board Hardware

Microcontroller Pin	Microcontroller Assignment	To Isolate, Remove...
Pin 16 PG3	Up switch	JP1
Pin 17 PG2/PWM0	User LED	JP2
Pin 26 PA0/U0RX	Virtual COM port receive	JP4

Table 2-2. Isolating On-Board Hardware (Continued)

Microcontroller Pin	Microcontroller Assignment	To Isolate, Remove...
Pin 29 PA3/SSI0FSS	OLED display chip select	JP5
Pin 37 PG6/PHA1	Right switch	JP6
Pin 36 PG7/PHB1	Select switch	JP7
Pin 40 PG5	Left switch	JP8
Pin 41 PG4	Down switch	JP9
Pin 31 PA5/SSI0TX	OLED display data in	JP10
Pin 28 PA2/SSI0CLK	OLED display clock	JP11
Pin 34 PA6/I2C1SCL	OLED display data/control select	JP12
Pin 27 PA1/U0TX	Virtual COM port transmit	JP13
Pin 86 PH0/PWM2	Sound+	JP14
Pin 85 PH1/PWM3	Sound-	JP15

Interfacing to the EVB

An array of accessible I/O signals makes it easy to interface the EVB to external circuits. All LM3S1968 I/O lines (except those with both JTAG and SWD functions) are brought out to 0.1" pitch pads. For quick reference, silk-screened labels on the PCB show primary pin functions.

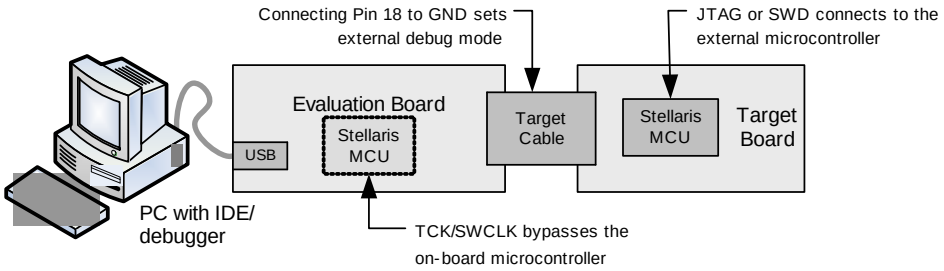
Table B-2 on page 28 has a complete list of I/O signals as well as recommended connectors.

Most LM3S1968 I/O signals are +5-V tolerant. Refer to the LM3S1968 data sheet for detailed electrical specifications.

Using the In-Circuit Debugger Interface

The Stellaris LM3S1968 Evaluation Kit can operate as an In-Circuit Debugger Interface (ICDI). ICDI acts as a USB to the JTAG/SWD adaptor, allowing debugging of any external target board that uses a Stellaris microcontroller. See "Debugging Modes" on page 12 for a description of how to enter Debug Out mode.

Figure 2-1. ICD Interface Mode



The debug interface operates in either serial-wire debug (SWD) or full JTAG mode, depending on the configuration in the debugger IDE.

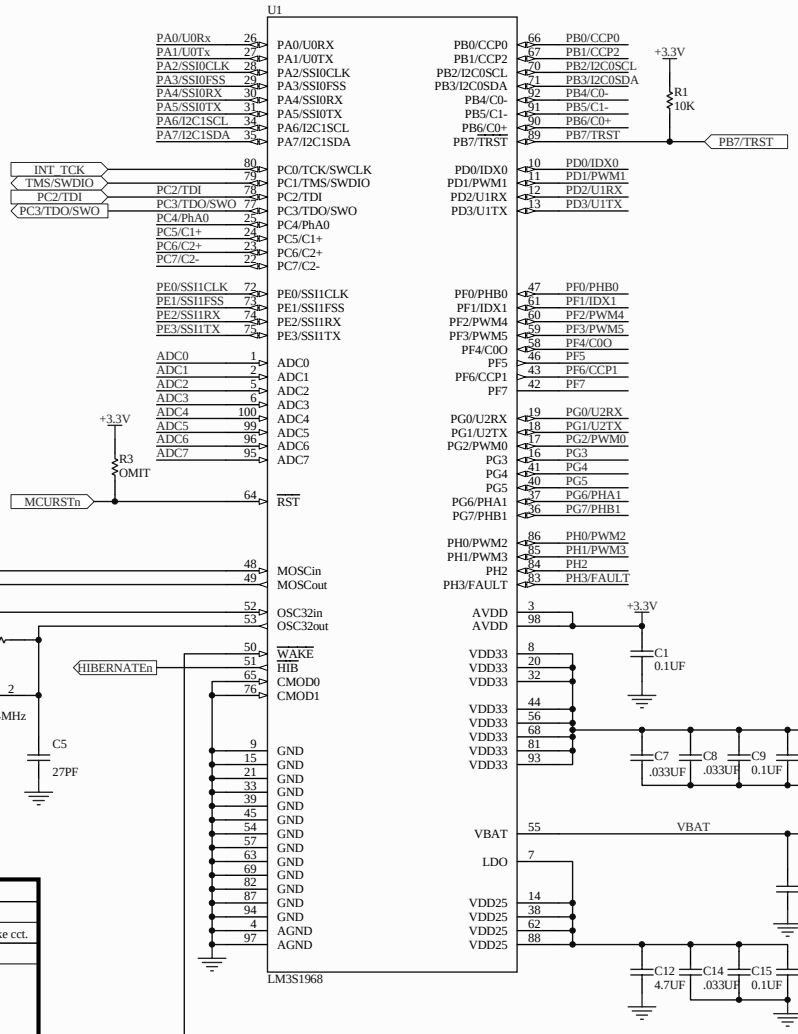
The IDE/debugger does not distinguish between the on-EVB Stellaris microcontroller and an external Stellaris microcontroller. The only requirement is that the correct Stellaris device is selected in the project configuration.

APPENDIX A

Schematics

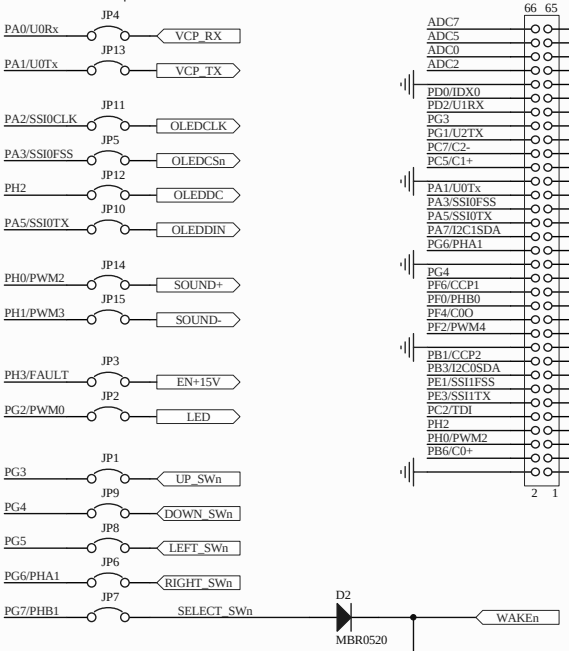
Schematics for the Stellaris LM3S1968 Evaluation Board follow.

Stellaris LM3S1968 Microcontroller

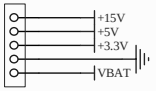


On-board Peripheral Signals

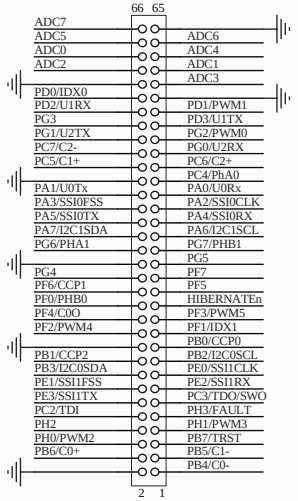
Jumpers can be cut to
free GPIO lines as required.



Power Break-out Header



I/O Break-out Header



History

Revision	Date	Description
0	8/9/07	Final prototype release
A	8/13/07	Production release with simplified wake cct.
B	3/3/07	Add TVCC control to debug circuit.

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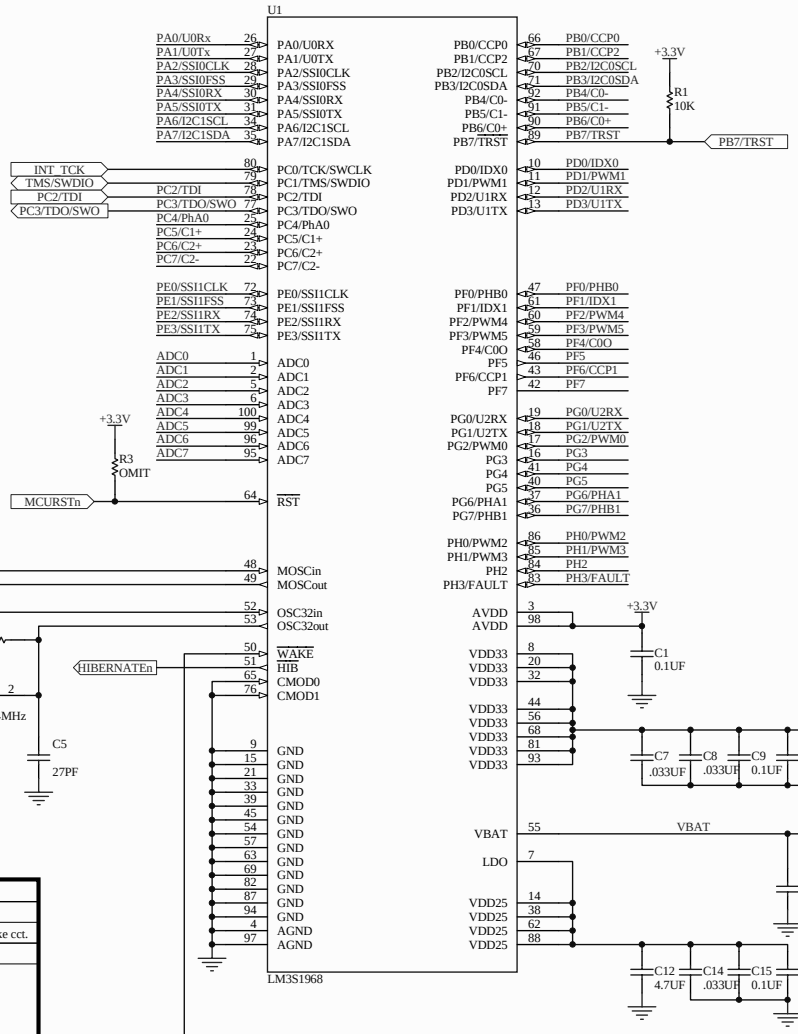
Drawing Title:	Stellaris LM3S1968 Evaluation Board	
Page Title:	LM3S1968 Microcontroller	
Size: B	Document Number: EK-LM3S1968	
Date: 3/4/2008	Sheet 1 of 4	Rev B

Stellaris LM3S1968 Microcontroller



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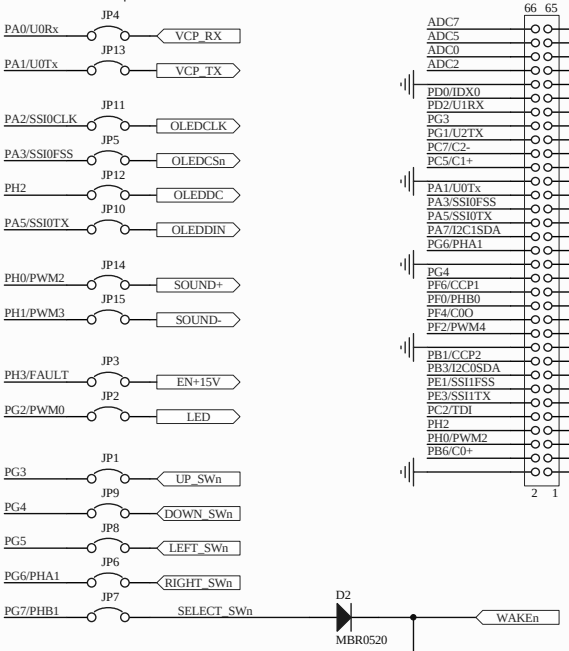
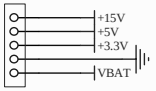
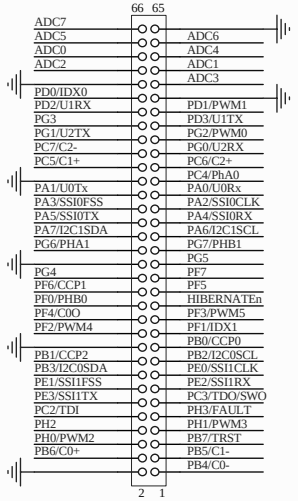


Power Break-out Header



I/O Break-out Header



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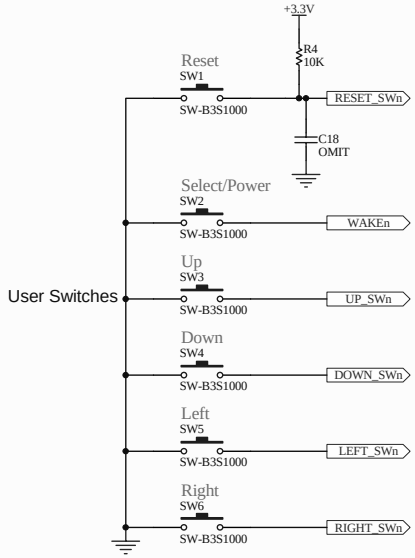
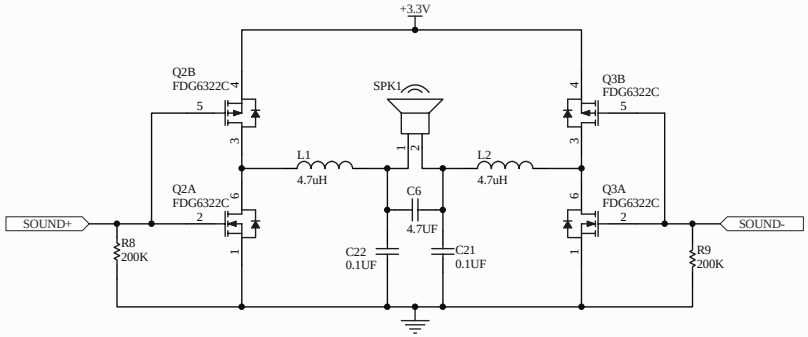
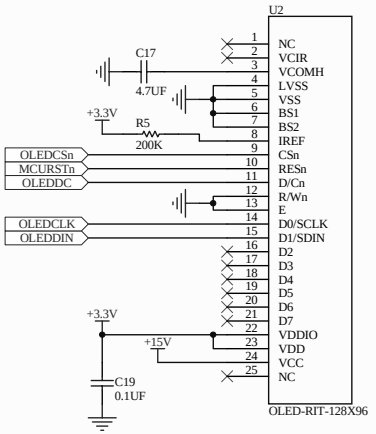
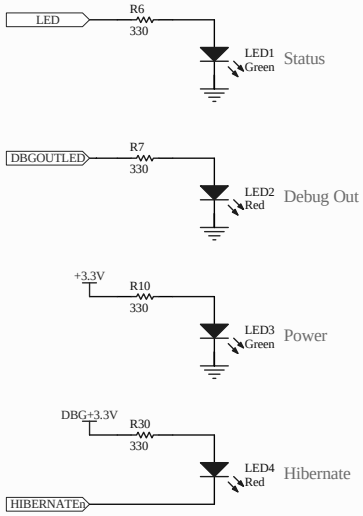




0.2W Audio Amplifier



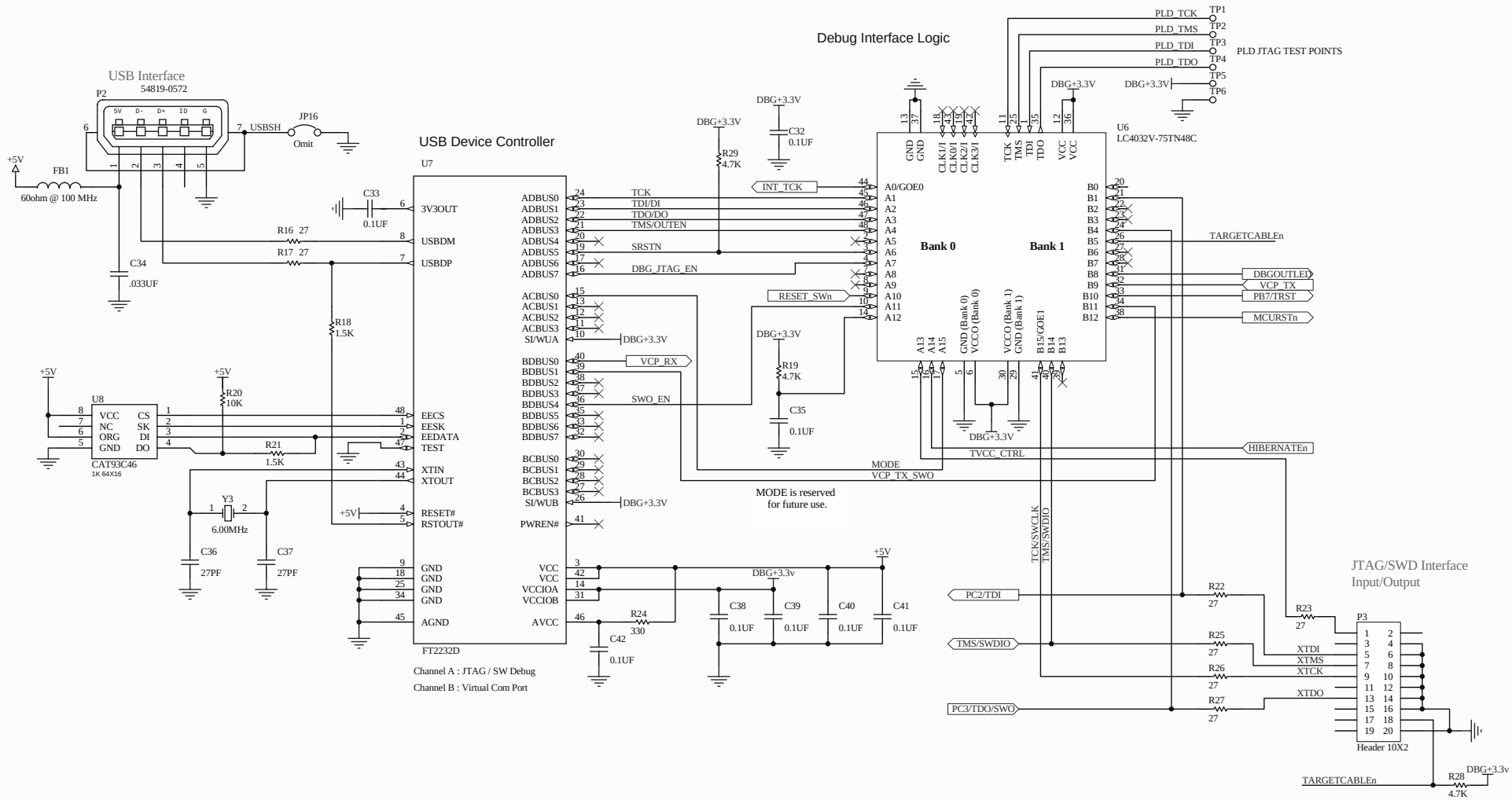
128x96 OLED Graphics Display



Status LEDs

LUMINARY MICRO

Drawing Title:	Stellaris LM3S1968 Evaluation Board
Page Title:	OLED Display, Switches and Audio
Size: B	Document Number: EK-LM3S1968
Date: 3/4/2008	Sheet 2 of 4 — Rev B


Debug Interface Logic
USB Interface
54819-0572
P2
JP16
Omit
USBSH
+5V
FB1
60ohm @ 100 MHz
C34
.033UF
C33
0.1UF
R16 27
R17 27
R18
1.5K
USB Device Controller
U7
3V3OUT
USBDM
USBDP
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
SI/WUA
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
SI/WUB
PWREN#
EECS
EESK
EEDATA
TEST
XTIN
XTOUT
RESET#
RSTOUT#
GND
VCC
VCCIOA
VCCIOB
AVCC
FT2232D
Channel A : JTAG / SW Debug
Channel B : Virtual Com Port
TCK
TDI/DI
TDO/DO
TMS/OUTEN
SRSTN
DBG_JTAG_EN
VCP_RX
SWO_EN
DBG+3.3V
R29
4.7K
C32
0.1UF
INT_TCK
RESET_SWn
R19
4.7K
C35
0.1UF
MODE
VCP_TX_SWO
MODE is reserved
for future use.
U8
CAT93C46
1K 64X16
R20
10K
R21
1.5K
Y3
6.00MHz
C36
27PF
C37
27PF
R24
330
C38
C39
C40
C41
C42
0.1UF
U6
LC4032V-75TN48C
Bank 0
Bank 1
A0/GOE0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
B10
B11
B12
TCK
TMS
TDI
TDO
VCC
GND
CLK1/I
CLK0/I
CLK2/I
CLK3/I
GND (Bank 0)
VCCO (Bank 0)
VCCO (Bank 1)
GND (Bank 1)
B15/GOE1
B14
B13
A13
A14
A15
TVCC_CTRL
HIBERNATEn
TARGETCABLEn
DBGOUTLED
VCP_TX
PB7/TRST
MCURSTn
PLD_TCK
PLD_TMS
PLD_TDI
PLD_TDO
TP1
TP2
TP3
TP4
TP5
TP6
PLD JTAG TEST POINTS
JTAG/SWD Interface
Input/Output
TCK/SWCLK
TMS/SWDIO
PC2/TDI
TMS/SWDIO
PC3/TDO/SWO
R22
R23
R25
R26
R27
27
P3
XTDI
XTMS
XTCK
XTDO
Header 10X2
R28
4.7K
DBG+3.3v
LUMINARY MICRO
Drawing Title: Stellaris LM3S1968 Evaluation Board
Page Title: USB and Debugger Interfaces
Size B
Document Number: EK-LM3S1968
Date: 3/4/2008
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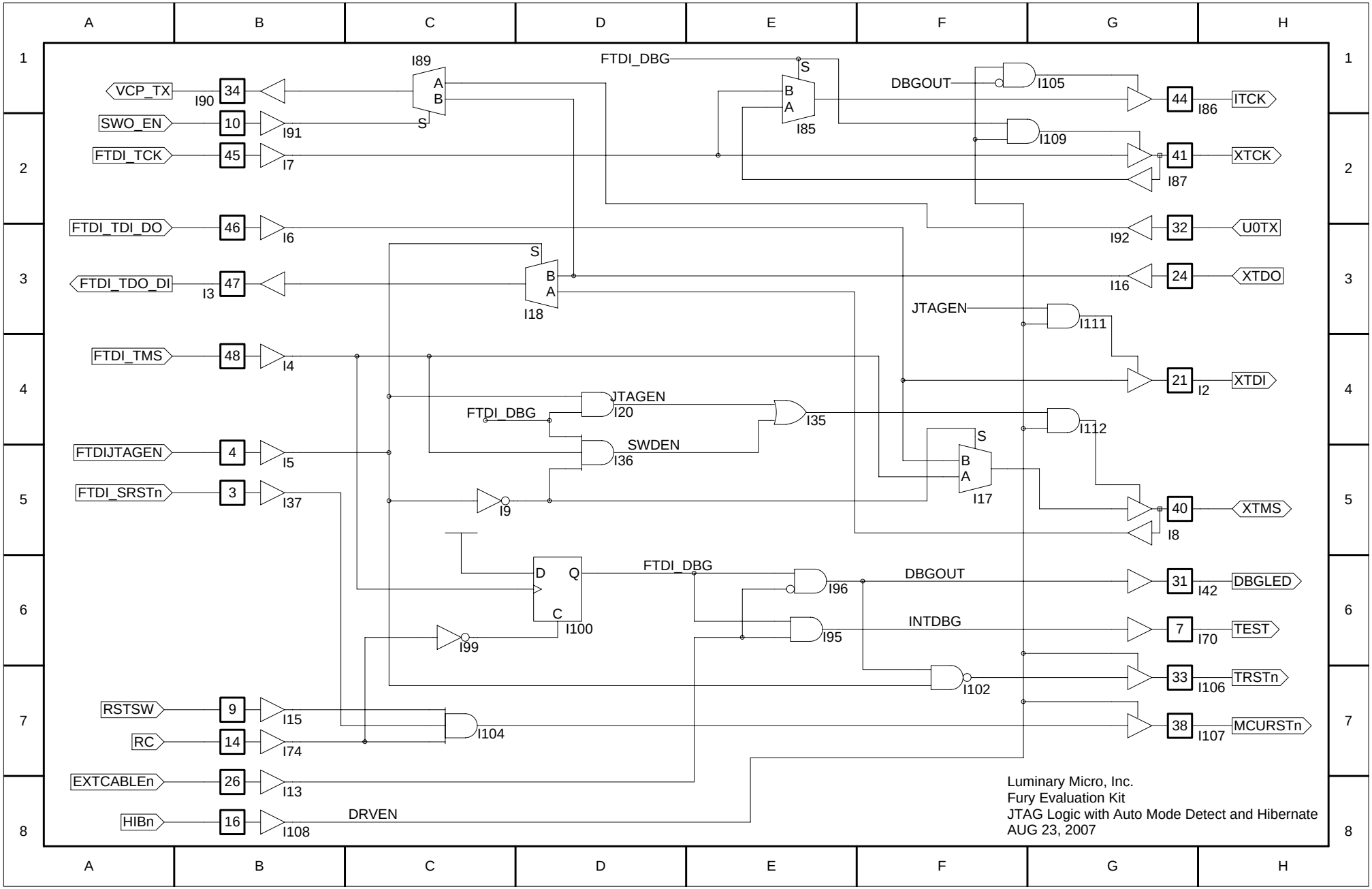

VCP_TX
34
I90
SWO_EN
10
I91
FTDI_TCK
45
I7
FTDI_TDI_DO
46
I6
FTDI_TDO_DI
47
I3
FTDI_TMS
48
I4
FTDIJTAGEN
4
I5
FTDI_SRSTn
3
I37
RSTSW
9
I15
RC
14
I74
EXTCABLEn
26
I13
HIBn
16
I108
I89
A
B
S
I18
I104
FTDI_DBG
S
B
A
I85
DBGOUT
I105
I109
44
I86
ITCK
41
I87
XTCK
I92
32
U0TX
I16
24
XTDO
JTAGEN
I111
21
I2
XTDI
I20
I35
I112
SWDEN
I36
I17
I9
40
I8
XTMS
D
Q
C
I100
I99
I96
I95
I102
INTDBG
31
I42
DBGLED
7
I70
TEST
33
I106
TRSTn
38
I107
MCURSTn
DRVEN
Luminary Micro, Inc.
Fury Evaluation Kit
JTAG Logic with Auto Mode Detect and Hibernate
AUG 23, 2007

A P P E N D I X B

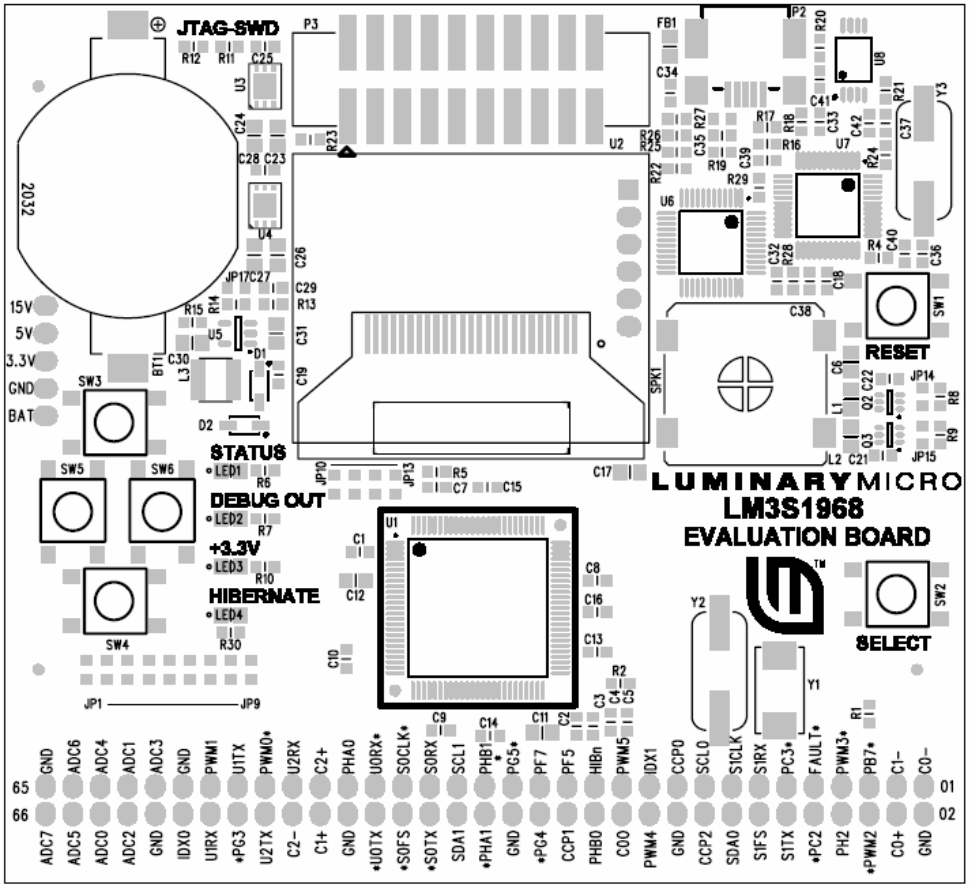
Connection Details

This appendix contains the following sections:

- Component Locations
- Evaluation Board Dimensions
- I/O Breakout Pads
- ARM Target Pinout
- References

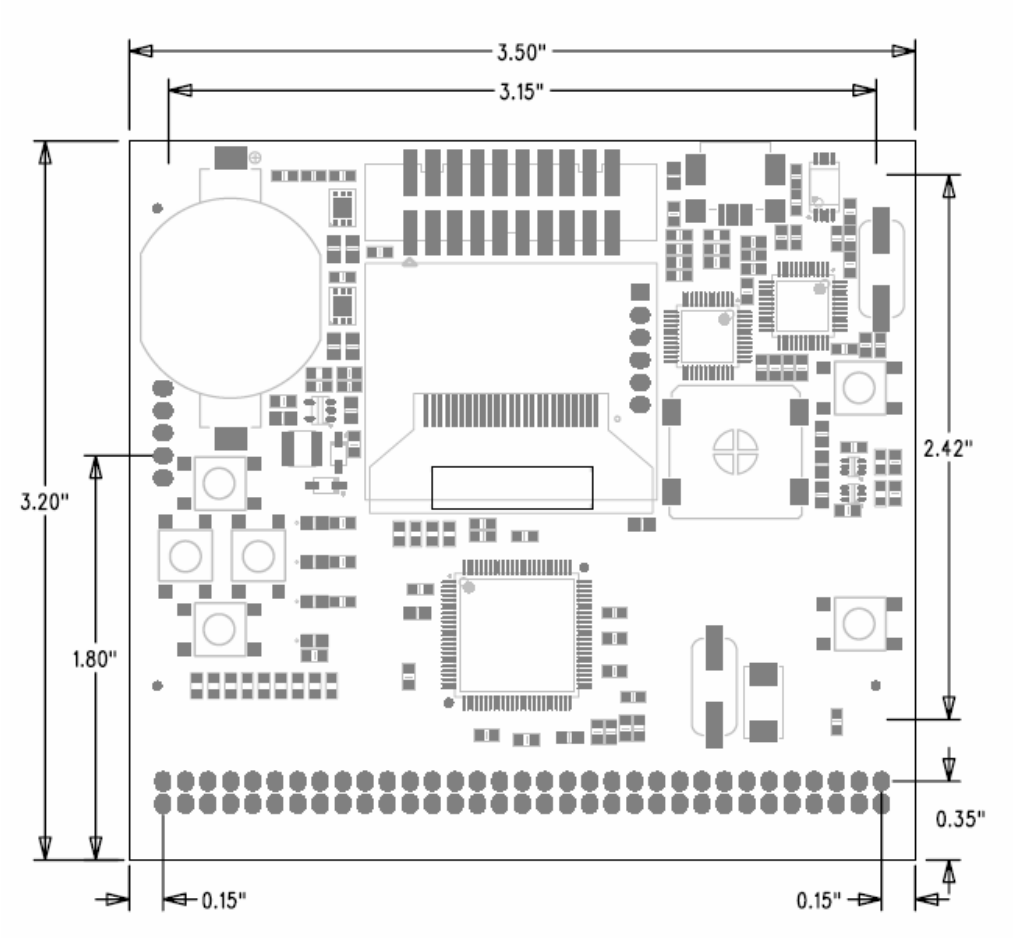
Component Locations

Figure B-1. Component Locations



Evaluation Board Dimensions

Figure B-2. LM3S1968 Evaluation Board Dimensions



I/O Breakout Pads

The LM3S1968 EVB has 58 I/O pads, 13 power pads, and 1 control connection, for a total of 71 pads. Connection can be made by soldering wires directly to these pads, or by using 0.1” pitch headers and sockets.

Note: In Table B-1, an asterisk (*) by a signal name (also on the EVB PCB) indicates the signal is normally used for on-board functions. Normally, you should cut the associated jumper (JP1-15) before using an assigned signal for external interfacing.

Table B-1. I/O Breakout Pads

Description	Pad No.	Description	Pad No.	Description	Pad No.	Description	Pad No.
PB4/C0-	1	PB1/CCP2	18	PA6/I2C1SCL	35	PG3*	52
GND	2	PB0/CCP0	19	PA7/I2C1SDA	36	PD1/PWM1	53
PB5/C1-	3	GND	20	PA4/SSI0RX	37	PD2/U1RX	54
PB6/C0+	4	PF1/IDX1	21	PA5/SSI0TX*	38	GND	55
PB7/TRST	5	PF2/PWM4	22	PA2/SSI0CLK*	39	PD0/IDX0	56
PH0/PWM2*	6	PF3/PWM5	23	PA3/SSI0FSS*	40	ADC3	57
PH1/PWM3*	7	PF4/C0O	24	PA0/U0RX*	41	GND	58
PH2*	8	HIBn	25	PA1/U0TX*	42	ADC1	59
PH3/FAULT*	9	PF0/PHB0	26	PC4/PhA0	43	ADC2	60
PC2/TDI	10	PF5	27	GND	44	ADC4	61
PC3/TDO/SWO	11	PF6/CCP1	28	PC6/C2+	45	ADC0	62
PE3/SSI1TX	12	PF7	29	PC5/C1+	46	ADC6	63
PE2/SSI1RX	13	PG4*	30	PG0/U2RX	47	ADC5	64
PE1/SSI1FSS	14	PG5*	31	PC7/C2-	48	GND	65
PE0/SSI1CLK	15	GND	32	PG2/PWM0*	49	ADC7	66
PB3/I2C0SDA	16	PG7/PHB1*	33	PG1/U2TX	50		
PB2/I2C0SCL	17	PG6/PHA1*	34	PD3/U1TX	51		

Recommended Connectors

Connection can be made by soldering wires directly to pads or using 0.1” pitch headers and sockets.

Table B-2. Recommended Connectors

Pins 1-66 (2 x 33 way)	PCB Socket	Sullins PPPC332LFBN-RC	Digikey S7136-ND
	Pin Header	Sullins PEC20DAAN	Digikey S2012E-20-ND

ARM Target Pinout

In ICDI input and output mode, the Stellaris LM3S1968 Evaluation Kit supports ARM’s standard 20-pin JTAG/SWD configuration. The same pin configuration can be used for debugging over serial-wire debug (SWD) and JTAG interfaces. The debugger software, running on the PC, determines which interface protocol is used.

The Stellaris target board should have a 2x10 0.1” pin header with signals as indicated in Table B-3. This applies to both an external Stellaris microcontroller target (Debug Output mode) and to external JTAG/SWD debuggers (Debug Input mode).

Table B-3. 20-Pin JTAG/SWD Configuration

Function	Pin	Pin	Function
VCC (optional)	1	2	nc
nc	3	4	GND
TDI	5	6	GND
TMS	7	8	GND
TCK	9	10	GND
nc	11	12	GND
TDO	13	14	GND
nc	15	16	GND
nc	17	18	GND
nc	19	20	GND

ICDI does not control $\overline{\text{RST}}$ (device reset) or $\overline{\text{TRST}}$ (test reset) signals. Both reset functions are implemented as commands over JTAG/SWD, so these signals are not necessary.

It is recommended that connections be made to all GND pins; however, both targets and external debug interfaces must connect pin 18 and at least one other GND pin to GND.

References

In addition to this document, the following references are included on the Stellaris Family Development Kit documentation CD-ROM and are also available for download at www.luminarymicro.com:

- *Stellaris LM3S1968 Evaluation Kit Quickstart Guide* for appropriate tool kit (see “Evaluation Kit Contents,” on page 9)
- *Stellaris LM3S1968 Read Me First* for the CAN Evaluation Kit
- Stellaris Family Peripheral Driver Library
- *Stellaris Family Peripheral Driver Library User’s Manual*, publication PDL-LM3S1968
- *Stellaris LM3S1968 Data Sheet*, publication DS-LM3S1968

Additional references include:

- *Solomon Systech SSD0323-OLED Controller Datasheet*
- *Future Technology Devices Incorporated FT2232C Datasheet*
- Information on development tool being used:
  - RealView MDK web site, www.keil.com/arm/rvmdkkit.asp
  - IAR Embedded Workbench web site, www.iar.com
  - Code Sourcery GCC development tools web site, www.codesourcery.com/gnu_toolchains/arm
  - Code Red Technologies development tools web site, www.code-red-tech.com

A P P E N D I X C

Contact Information

Company Information

Luminary Micro, Inc. designs, markets, and sells ARM Cortex-M3-based microcontrollers (MCUs). Austin, Texas-based Luminary Micro is the lead partner for the Cortex-M3 processor, delivering the world's first silicon implementation of the Cortex-M3 processor. Luminary Micro's introduction of the Stellaris® family of products provides 32-bit performance for the same price as current 8- and 16-bit microcontroller designs. With entry-level pricing at $1.00 for an ARM technology-based MCU, Luminary Micro's Stellaris product line allows for standardization that eliminates future architectural upgrades or software tool changes.

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